



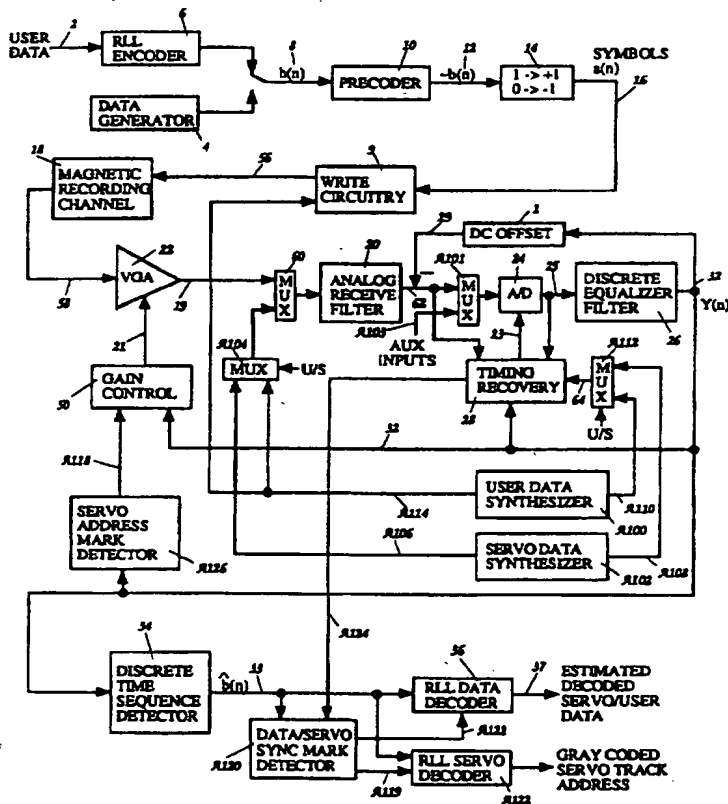
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(54) Title: IMPROVED FAULT TOLERANT SYNC MARK DETECTOR FOR SAMPLED AMPLITUDE MAGNETIC RECORDING

(57) Abstract

A sampled amplitude read channel reads data from a magnetic medium by detecting digital data from a sequence of discrete time sample values generated by sampling pulses in an analog read signal from a read head positioned over the magnetic medium. The digital data comprises a preamble field followed by a sync mark followed by a data field. Timing recovery (28) in the read channel synchronizes to a phase and frequency of the preamble field and a sync detector (A120) detects the sync mark in order to frame operation of an RLL decoder (36, A122) for decoding the detected data field. To decrease the probability of early misdetection, the sync mark is chosen to have minimum correlation with shifted versions of the sync mark concatenated with the preamble field. To further increase the fault tolerance, the sync mark detector is enabled by timing recovery relative to the end of the preamble field. A timing recovery state machine generates expected sample values used to acquire the preamble field, and a current state of the state machine indicates when the preamble ends relative to a predetermined clock interval. As a result, the search for an appropriate sync mark need only look for minimum correlation during shifts at the predetermined clock interval, thereby increasing the fault tolerant characteristic of the sync mark. In one embodiment, both the sign and magnitude of the data are used in the correlation to further increase the fault tolerance.



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IMPROVED FAULT TOLERANT SYNC MARK DETECTOR FOR SAMPLED AMPLITUDE MAGNETIC RECORDING

FIELD OF INVENTION

The present invention relates to the control of magnetic storage systems for digital computers, and particularly, to a sampled amplitude read channel incorporating a fault tolerant sync mark detector.

CROSS REFERENCE TO RELATED APPLICATIONS AND PATENTS

This application is related to other co-pending U.S. patent applications, namely application serial numbers 08/341,251 entitled "Sampled Amplitude Read Channel Comprising Sample Estimation Equalization, Defect Scanning, Channel Quality, Digital Servo Demodulation, PID Filter for Timing Recovery, and DC Offset Control," 08/313,491 entitled "Improved Timing Recovery For Synchronous Partial Response Recording." This application is also related to several U.S. patents, namely U.S. Pat. No. 5,359,631 entitled "Timing Recovery Circuit for Synchronous Waveform Sampling," 5,291,499 entitled "Method and Apparatus for Reduced-Complexity Viterbi-Type Sequence Detectors," 5,297,184 entitled "Gain Control Circuit for Synchronous Waveform Sampling," 5,329,554 entitled "Digital Pulse Detector," and 5,424,881 entitled "Synchronous Read Channel." All of the above-named patent applications and patents are assigned to the same entity, and all are incorporated herein by reference.

BACKGROUND OF THE INVENTION

In magnetic disk storage systems for computers, digital data serves to modulate the current in a read/write head coil so that a sequence of corresponding magnetic flux transitions are written onto the surface of a magnetic medium in concentric tracks. To read this recorded data, the read/write head passes over the magnetic medium and transduces the magnetic transitions into pulses in an analog signal that alternate in polarity. These pulses are then detected and decoded by read channel circuitry to reproduce the digital

data.

Detecting and decoding the pulses into a digital sequence can be performed by a simple peak detector in a conventional analog read channel or, as in more recent designs, by a discrete time sequence detector in a sampled amplitude read channel. Discrete time sequence detectors are preferred over simple analog pulse detectors because they compensate for intersymbol interference (ISI) and, therefore, are less susceptible to noise. As a result, discrete time sequence detectors increase the capacity and reliability of the storage system.

There are several well known discrete time sequence detection methods including discrete time pulse detection (DPD), partial response (PR) with Viterbi detection, maximum likelihood sequence detection (MLSD), decision-feedback equalization (DFE), enhanced decision-feedback equalization (EDFE), and fixed-delay tree-search with decision-feedback (FDTS/DF).

In conventional peak detection schemes, analog circuitry, responsive to threshold crossing or derivative information, detects peaks in the continuous time analog signal generated by the read head. The analog read signal is "segmented" into bit cell periods and interpreted during these segments of time. The presence of a peak during the bit cell period is detected as a "1" bit, whereas the absence of a peak is detected as a "0" bit. The most common errors in detection occur when the bit cells are not correctly aligned with the analog pulse data. Timing recovery, then, adjusts the bit cell periods so that the peaks occur in the center of the bit cells on average in order to minimize detection errors. Since timing information is derived only when peaks are detected, the input data stream is normally run length limited (RLL) to limit the number of consecutive "0" bits.

As the pulses are packed closer together on the concentric data tracks in the effort to increase data density, detection errors can also occur due to intersymbol interference, a distortion in the read signal caused by closely spaced overlapping pulses. This interference can cause a peak to shift out of its bit cell, or its magnitude to decrease, resulting in a detection error. The ISI effect is reduced by decreasing the data density or by employing an encoding scheme to ensure that a minimum number of "0" bits occur

between "1" bits. For example, a (d,k) run length limited (RLL) code constrains to d the minimum number of "0" bits between "1" bits, and to k the maximum number of consecutive "0" bits. A typical RLL code is a $(1,7)$ $2/3$ rate code which encodes 8 bit data words into 12 bit codewords to satisfy the $(1,7)$ constraint.

Sampled amplitude detection, such as partial response (PR) with Viterbi detection, allows for increased data density by compensating for intersymbol interference. Unlike conventional peak detection systems, sampled amplitude recording detects digital data by interpreting, at discrete time instances, the actual value of the pulse data. The analog pulses are sampled at the baud rate (code bit rate) and the digital data is detected from these discrete time sample values. A discrete time sequence detector, such as a Viterbi detector, interprets the discrete time sample values in context to determine a most likely sequence for the data. In this manner, the effect of ISI can be taken into account during the detection process, thereby decreasing the probability of a detection error. This increases the effective signal to noise ratio and, for a given (d,k) constraint, allows for significantly higher data density as compared to conventional analog peak detection read channels.

The application of sampled amplitude techniques to digital communication channels is well documented. See Y. Kabal and S. Pasupathy, "Partial Response Signaling", IEEE Trans. Commun. Tech., Vol. COM-23, pp.921-934, Sept. 1975; and Edward A. Lee and David G. Messerschmitt, "Digital Communication", Kluwer Academic Publishers, Boston, 1990; and G.D. Forney, Jr., "The Viterbi Algorithm", Proc. IEEE, Vol. 61, pp. 268-278, March 1973.

Applying sampled amplitude techniques to magnetic storage systems is also well documented. See Roy D. Cideciyan, Francois Dolivo, Walter Hirt, and Wolfgang Schott, "A PRML System for Digital Magnetic Recording", IEEE Journal on Selected Areas in Communications, Vol. 10 No. 1, January 1992, pp.38-56; and Wood et al, "Viterbi Detection of Class IV Partial Response on a Magnetic Recording Channel", IEEE Trans. Commun., Vol. Com-34, No. 5, pp. 454-461, May 1986; and Coker et al, "Implementation of PRML in a Rigid Disk Drive", IEEE Trans. on Magnetics, Vol. 27, No. 6, Nov. 1991; and

Carley et al, "Adaptive Continuous-Time Equalization Followed By FDTS/DF Sequence Detection", Digest of The Magnetic Recording Conference, August 15-17, 1994, pp. C3; and Moon et al, "Constrained-Complexity Equalizer Design for Fixed Delay Tree Search with Decision Feedback", IEEE Trans. on Magnetics, Vol. 30, No. 5, Sept. 1994; and Abbott et al, "Timing Recovery For Adaptive Decision Feedback Equalization of The Magnetic Storage Channel", Globecom'90 IEEE Global Telecommunications Conference 1990, San Diego, CA, Nov. 1990, pp.1794-1799; and Abbott et al, "Performance of Digital Magnetic Recording with Equalization and Offtrack Interference", IEEE Transactions on Magnetics, Vol. 27, No. 1, Jan. 1991; and Cioffi et al, "Adaptive Equalization in Magnetic-Disk Storage Channels", IEEE Communication Magazine, Feb. 1990; and Roger Wood, "Enhanced Decision Feedback Equalization", Intermag'90.

The format of the data stored on the magnetic disk, as shown in Figure 2A and 2B, is similar for both peak detection and sampled amplitude read channels. The data is stored as a series of concentric tracks 13 each comprising a number of user data sectors 15 and embedded servo data sectors 17. As illustrated in Figure 2A, the embedded servo data sectors 17 are recorded at the same data rate across the disk's radius. For the user data sectors 15, however, the disk is partitioned into a number of zones (e.g., an outer zone 11 and an inner zone 27) and the data rate increased in the outer zones in order to achieve a more constant linear bit density. This "zoned" recording technique allows more data to be stored in the outer diameter tracks, thereby increasing the overall capacity of the disk.

Figure 2B shows the format of a user data sector 15 and a servo data sector 17 comprising a preamble (68,5), sync mark (70,7) and data field (72,3). The read channel processes the preamble (68,5) to adjust the magnitude of the read signal (and synchronize timing recovery in sampled amplitude read channels) so that it can accurately read the data field (72,3). The sync mark (70,7) demarks the beginning of the data field (72,3), and when the read channel detects the sync mark (70,7), it signals a disk controller (not shown) to begin processing the detected data.

The sync mark (70,7) must be detected at the correct time or the read channel

cannot synchronize to the data field (72,3). Errors due to noise in the system can cause the read channel to detect the sync mark (70,7) too early or fail to detect it altogether. That is, errors in the detected read signal can cause the read channel to falsely detect the sync mark as the end of the preamble concatenated with the beginning of the sync mark. When this happens, error detection circuitry within the disk controller will recognize that the sync mark was falsely detected and initiate a re-try. The storage system will wait for the disk to complete a revolution, which increases the overall access time, and again attempt to accurately detect the sync mark.

A sync detector in the read channel detects the sync mark (70,7) by correlating a target sync mark with the bit sequence detected from the read signal. In order to minimize the probability of early misdetection, the sync mark (70,7) is selected to have a minimum correlation with the sync mark (70,7) concatenated with the preamble (68,5). It is also selected for maximum probability of correct detection when the sync mark is corrupted by errors due to noise. This is accomplished with a computer search program which searches for an appropriate sync mark by correlating a target sync mark with shifted values of the target sync mark appended to the preamble. The search program also correlates the target sync mark with corrupted versions of the sync mark appended to the preamble. Selecting a sync mark to have minimum correlation with the preamble increases the fault tolerance of the sync mark detector.

Prior art sync mark detectors do not use the preamble (68,5) to assist in detecting the sync mark (70,7). Instead, conventional sync mark detectors execute a correlation with each new bit detected from the read signal. For example, U.S. Patent No. 5,384,671 issued to Fisher discloses a sync mark detection technique that selects a sync mark to have minimum correlation with the preamble but does not use information from the preamble in the detection process. Furthermore, prior art sync mark detectors do not use the sign of the sampled data in order to improve the correlation sensitivity.

What is needed is a sync mark detection technique that uses information from the preamble and sign of the sampled data in order to further increase the fault tolerance of the sync mark detector.

SUMMARY OF THE INVENTION

In a storage device for storing digital data on a magnetic disk in a series of concentric tracks comprising a number of user data sectors and embedded servo data sectors where each sector comprises a preamble, sync mark and data field, a sampled amplitude read channel employs a fault tolerant sync mark detector that uses information from the preamble to improve the sync mark detection process. A state machine generates expected sample values used by a timing recovery circuit to acquire the preamble field. The preamble is recorded to the disk in a manner that ensures the state machine will be in a predetermined state when the end of the preamble is encountered. In this manner, the sync mark detector need only execute a correlation of the detected bit sequence with a target sync mark when the state machine is in the predetermined state.

As the bit sequence is detected from the read signal with each new sample period, it is shifted into a shift register. The sync mark detector correlates the detected bit sequence with a target sync mark and outputs a sync mark detected signal when the sync mark is found. The output of the sync mark detector is enabled according to the current state of the state machine, i.e., at a predetermined sample period interval. In one example embodiment, the end of preamble can occur only when the state machine is in two of four states. Therefore, the sync detector is enabled at every other sample period. In another embodiment, the sync mark detector processes the even and odd interleaves of the detected bit sequence in parallel, and the current state of the state machine initializes the sync mark detector rather than enable its output.

In both of these embodiments, the sync mark detector's output represents the correlation of the bit sequence with the target sync mark only during a predetermined sample period interval. This increases the fault tolerance of the sync mark detector and the fault tolerant characteristics of the sync mark itself by allowing the computer search program to search for a sync mark having minimum correlation with the preamble at the predetermined interval.

The present invention achieves further fault tolerance by minimizing a mean

squared error between a partial response representation of the detected sync mark and the target sync mark. This increases the correlation sensitivity since a partial response signal provides both sign and magnitude information. The read channel's discrete time sequence detector outputs a sign and magnitude of estimated sample values corresponding to a PR4 representation of the detected digital data. For read channels employing PR4 sequence detectors, the PR4 sync mark data is generated by appending a sign bit to the detected binary sequence and normalizing the PR4 values from $(-2,0,+2)$ to $(-1,0,-1)$. For EPR4 and EEPR4 sequence detectors, the PR4 sync mark data is generated by appending a sign bit to the detected binary sequence (NRZI data) and then encoding the signed NRZI data into a PR4 representation.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a block diagram of a conventional sampled amplitude recording channel.

Figure 2A shows an exemplary data format of a magnetic disk having a plurality of concentric tracks recorded in zones at varying data rates where each track contains a plurality of user data and embedded servo data sectors.

Figure 2B shows an exemplary format of a user data sector and an embedded servo data sector.

Figure A3 is a block diagram of the sampled amplitude read channel of the present invention comprising automatic gain control, DC offset control, timing recovery, a first and second synthesizer for processing user and servo data respectively, an asynchronous servo address mark detector, and a sync mark detector for detecting user data and servo data sync marks.

Figure C3 is a block diagram of a sampled amplitude read channel timing recovery circuit comprising a VFO for generating a sampling frequency.

Figure C4 shows more details of the data/servo sync detector and particularly the operation with respect to the timing recovery control signal.

Figure C5A shows the acquisition read signal with corresponding actual and

estimated sample values.

Figure C5B is a detailed diagram of the preferred embodiment for the expected sample value generator and phase error detector used in the timing recovery circuit.

Figure C6 is an alternative embodiment for the data/servo sync detector which processes the even and odd interleaves of the read signal in parallel.

Figure C7 shows an EPR4 or EEPR4 sequence detector having a signed NRZI to PR4 data encoder.

Figure C8 shows an implementation of a sync mark detector that compares a PR4 representation of the detected sync mark with the target sync mark.

Figure C9 shows yet another implementation of the sync mark detector having a preamble synthesizer for generating an enable and sign control signals in response to the recorded preamble.

Figure C10 shows an implementation of the preamble synthesizer of Figure C9.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

Conventional Sampled Amplitude Read Channel

Figure 1 is a detailed block diagram of a conventional sampled amplitude read channel. During a write operation, either user data 2 or preamble data from a data generator 4 (for example 2T preamble data) is written onto the media. An RLL encoder 6 encodes the user data 2 into a binary sequence $b(n)$ 8 according to an RLL constraint. For PR4 read channels, a precoder 10 precodes the binary sequence $b(n)$ 8 in order to compensate for the transfer function of the recording channel 18 and equalizing filters to form a precoded sequence $\sim b(n)$ 12. The precoded sequence $\sim b(n)$ 12 is converted into symbols $a(n)$ (or NRZ data) 16 by translating $\sim b(N) = 0$ into $a(N) = -1$, and $\sim b(N) = 1$ into $a(N) = +1$. Write circuitry 9 responsive to the symbols $a(n)$ 16 modulates the current in the recording head coil at the baud rate $1/T$ to record the binary sequence onto the media. A frequency synthesizer 52 provides a baud rate write clock 54 to the write circuitry 9. The recorded data is referred to as NRZI data where each magnetic transition represents a "1" bit and each non-transition represents a "0" bit.

When reading the recorded binary sequence from the media, timing recovery 28 is first locked to the write frequency by selecting, as the input to the read channel, the write clock 54 through a multiplexor 60. Once locked to the write frequency, the multiplexor 60 selects the signal 19 from the read head as the input to the read channel in order to acquire the acquisition preamble. A variable gain amplifier 22 adjusts the amplitude of the analog read signal 58, and an analog filter 20 provides initial equalization toward the desired response. A sampling device 24 samples the analog read signal 62 from the analog filter 20, and a discrete time filter 26 provides further equalization of the sample values 25 toward the desired response. In partial response recording, for example, the desired response is often selected from Table 1. A DC offset circuit 1 responsive to the equalized sample values 32 computes and subtracts the DC offset 29 from the analog read signal 62.

The equalized sample values 32 are applied to decision directed gain control 50 and timing recovery 28 for adjusting the amplitude of the read signal 58 and the frequency and phase of the sampling device 24, respectively. Timing recovery adjusts the frequency of sampling device 24 over line 23 in order to synchronize the equalized samples 32 to the baud rate. Frequency synthesizer 52 provides a coarse center frequency setting to the timing recovery circuit 28 over line 64 in order to center the timing recovery frequency over temperature, voltage, and process variations. Gain control 50 adjusts the gain of variable gain amplifier 22 over line 21. The equalized samples $Y(n)$ 32 are sent to a discrete time sequence detector 34, such as a maximum likelihood (ML) Viterbi sequence detector, to detect an estimated binary sequence $\hat{b}(n)$ 33. The discrete time sequence detector operates according to the selected equalization (PR4, EPR4, EEPR4, etc.), and for PR4 equalization, the preferred embodiment is two sliding threshold detectors for processing the even and odd interleaves, respectively.

An RLL decoder 36 decodes the estimated binary sequence $\hat{b}(n)$ 33 into estimated user data 37. A data sync mark detector 66 detects the sync mark 70 (shown in Figure 2B) in the data sector 15 in order to frame the operation of the RLL decoder 36 and signal the beginning of user data 72. In the absence of errors, the estimated binary

sequence $\hat{b}(n)$ 33 equals the recorded binary sequence $b(n)$ 8, and the decoded user data 37 equals the recorded user data 2.

Improved Sampled Amplitude Read Channel

Figure A3 is a block diagram of the improved sampled amplitude read channel of the present invention comprising a user data frequency synthesizer A100 and a servo data frequency synthesizer A102. When reading user data, a control line U/S selects the output A114 of the user data synthesizer A100 as the lock to reference frequency through a multiplexor A104. The control line U/S also selects the coarse center frequency setting A110 of the user data synthesizer A100 through multiplexor A112 as the timing recovery control signal 64. When the read channel switches into servo data mode in order to read a servo wedge, the control line U/S selects the output A106 of the servo data synthesizer A102 as the lock to reference frequency through multiplexor A104. The control line U/S also selects the coarse center frequency setting A108 from the servo data synthesizer A102 through multiplexor A112 as the timing recovery control signal 64.

The read channel further comprises an asynchronous servo address mark detector A126 for generating a control signal A118 indicating when the servo address mark has been detected. The servo address mark detector A126 switches operation of the gain control circuit over line A118 to compensate for the unpredictable amplitude fluctuations caused by the inter-track head position and the wide range of user to servo data densities.

A data/servo sync mark detector A120, responsive to the detected binary sequence 33 from the sequence detector 34, detects both user data and servo data sync marks and generates framing signals (A121, A119) to frame operation of a user data RLL decoder 36 and a servo data RLL decoder A122, respectively. The sync detector A120 is also responsive to a control signal A124 from the timing recovery circuit 28 to aid in the sync mark detection process.

The read channel further comprises auxiliary analog inputs for sampling other analog signals generated within the disk drive such as the driving current for a Voice Coil Motor in a servo system, or the output of a temperature sensor. A multiplexor A101

selects, as the input to sampling device 24, the analog read signal 62 from the analog receive filter 20 or one of a plurality of auxiliary input signals A103. When an auxiliary input is selected for sampling, the output 25 of the sampling device 24 is stored into registers for subsequent processing by a microcontroller such as a servo controller.

Data/Servo Sync Mark Detector

After acquiring the preamble (68,5) (shown in Figure 2B), a data/servo sync mark detector A120 of Figure A3 searches for the sync mark (70,7) which demarks the beginning of the user or servo data fields. When the sync mark (70,7) is detected, the data/servo sync detector A120 enables operation of the RLL data decoder 36 or the RLL servo decoder A122 in order to frame the user or servo data fields.

The data/servo sync mark detector A120 detects the sync mark (70,7) by correlating a target sync mark with the estimated bit sequence $b(n)$ 33 from the discrete time sequence detector. In order to minimize the probability of early misdetection, the sync mark (70,7) is selected to have a minimum correlation with the sync mark (70,7) concatenated with the preamble (68,5). It is also selected for maximum probability of correct detection when the sync mark is corrupted by errors due to noise. This is accomplished with a computer search program which searches for an appropriate sync mark by correlating a target sync mark with shifted values of the target sync mark appended to the preamble. The search program also correlates the target sync mark with corrupted versions of the sync mark appended to the preamble.

In a first embodiment of the present invention, operation of the correlation process is understood with reference to Figure C4. The estimated bit sequence $b(n)$ 33 is shifted into a shift register C100 and the target sync mark (servo or data) is loaded into register C102. Registers C100 and C102 are programmable to accommodate various sync mark lengths. The corresponding bits of registers C100 and C102 are correlated (using an exclusive-nor gate not shown) and summed with an adder C104. A threshold comparator C118 compares the output of the adder C104 to a predetermined programmable threshold and outputs a threshold correlation signal C106. The threshold correlation signal C106 is

enabled through an AND gate C108 by a control signal C194 generated in response to a timing recovery control signal A124. The output C114 of the AND gate C108 is applied to the RLL decoder framing signals (A121,A119) through a de-multiplexor C116 according to the state of the U/S control signal. The control signal C194 for enabling the threshold correlation signal C106 is understood in relation to the operation of the timing recovery circuit 28, an overview of which is provided in Figure C3.

In Figure C3, the output 23 of a variable frequency oscillator (VFO) B164 controls the sampling clock of a sampling device 24 which is typically an analog-to-digital converter (A/D) in digital read channels. A frequency error detector B157 and phase error detector B155 control the frequency of the VFO B164, and a loop filter B160 provides control over the closed loop characteristics. A multiplexor B159 may select the unequalized sample values 25 during acquisition, and the equalized sample values 32 during tracking. From the sample values received over line B149, the frequency error detector B157 generates a frequency error, and the phase error detector B155 generates a phase error. The phase error is also computed from expected sample values $X(n)$ from an expected sample generator B151 during acquisition, and estimated sample values $\hat{X}(n)$ from a sample value estimator B141, such as a slicer according to Table B2, during tracking.

Referring again to Figure 2B, before acquiring the acquisition preamble (68,5) the phase-lock-loop first locks onto a predetermined nominal sampling frequency according to the zone where the current track is located. In this manner, the phase-lock-loop is close to the desired acquisition frequency when it switches to acquisition mode. As previously mentioned, the acquisition preamble (68,5) is processed during acquisition mode in order to lock the PLL to the desired sampling phase and frequency before sampling the user or servo data fields (72,3). Once locked onto the acquisition preamble, the phase-lock-loop switches into tracking mode and, after detecting the sync mark (70,7), begins tracking user or servo data (72,3).

To record the acquisition preamble to the disk, a data generator 4 connected to the input of the precoder 10 outputs a series of "1" bits to generate a 2T training preamble sequence at the output of the precoder 10 of the form (1,1,0,0,1,1,0,0,1,1,0,0,...). This 2T

preamble maximizes the magnitude of a PR4 read channel, and during acquisition, it is "side sampled" to generate the following sample sequence:

$$(+A, +A, -A, -A, +A, +A, -A, -A, +A, +A, -A, -A, \dots).$$

Figure C5A shows the 2T preamble "side sampled" with the expected samples C120 in relation to the signal samples C122 and a corresponding phase error T. Figure C5B shows an implementation of the phase error detector B155 and the expected sample value generator B151 of Figure C3. To adjust the initial sampling timing phase, the phase error detector B155 computes a timing gradient which minimizes the mean squared error between read signal sample values and expected sample values. The timing gradient value \dot{y}_t C124 is computed as:

$$\dot{y}_t(n) = Y(n-1) \cdot X(n) - Y(n) \cdot X(n-1)$$

where $Y(n)$ are the read signal sample values B149 and $X(n)$ are the expected sample values C126.

Referring again to Figure C5B, the outputs (C137, C138) of a 2-bit counter C128 correspond to the expected "side sampled" preamble sequence:

00 \rightarrow +A, -A
 01 \rightarrow -A, -A,
 10 \rightarrow -A, +A
 11 \rightarrow +A, +A.

The expected sample value is scaled to $|A| = 1$ so that the multipliers (C130a, C130b) of the phase error detector B155 multiply by +1, -1 or 0. Thus, the expected sample values $X(n)$ C126 are two bits wide in order to represent the ternary values:

(00=0, 01=1, and 11=-1).

A multiplexor C132, responsive to the outputs (C137, C138) of the counter C128, selects the expected sample values $X(n)$ C126 which correspond to the current counter state.

The counter C128 is loaded C134 with an initial starting state by logic C136 in response to two consecutive sample values $Y(n)$ C149. The counter output bits C0 C138 and C1 C137 are initialized to:

$$C1 = \text{sgn}(Y(n-1)); \text{ and}$$

$$C0 = \text{sgn}(Y(n)) \text{ XOR } \text{sgn}(Y(n-1))$$

where $\text{sgn}(x)$ returns a 0 if x is positive and 1 if negative.

Table C2 shows the "side sampled" starting state values loaded into counter C128 corresponding to the two consecutive sample values.

After the counter C128 is loaded with the initial starting state, it sequences through the states according to the expected samples in the 2T preamble at each sample clock 23. The four possible sequences are:

(+A, -A, -A, +A, +A, -A, ...); and

(-A, -A, +A, +A, -A, -A, ...); and

(-A, +A, +A, -A, -A, +A, ...); and

(+A, +A, -A, -A, +A, +A, ...).

Using a counter to generate expected sample values avoids a "hang up" problem associated with the prior art, and, in addition, the state of the counter C128 can be advantageously used in the selection and detection of the sync mark (70,7).

If the 2T acquisition preamble (68,5) always ends with two positive samples ++ or two negative samples -- (e.g., samples C120d in Figure C5A), then the output 25 of the A/D converter 24 will be the last preamble sample only when the counter C128 of Figure C5B is in state (-A, -A) or (+A, +A) which corresponds to counter C128 outputs 01 (i.e., the count is one) or 11 (i.e., the count is three). Therefore, the output 25 of the A/D converter 24 will be the first sample of the sync mark only when the counter C128 output is 10 (i.e., the count is two) or 00 (i.e., the count is zero). Assuming the discrete time equalizing filter 26 and the discrete time sequence detector 34 of Figure A3 contain d bits of delay, then the output 33 of the sequence detector 34 will be the first bit of the sync mark only when the counter C128 output is $(2+d) \text{ MOD } 4$ or $(0+d) \text{ MOD } 4$. Finally, assuming the sync mark register C100 is k bits in length, then the sync mark will be completely loaded into the register C100 only when the counter C128 output is $(2+d+k) \text{ MOD } 4$ or $(0+d+k) \text{ MOD } 4$. Thus, the data/servo sync mark detector A120 is enabled only during these two counts, i.e., only at every other sample period. Counter decode logic C190 enables the output of the data/servo sync mark detector A120 through AND gate C108 only when the counter

C128 output (C137,C138) equals either of the two counts $(2+d+k) \text{ MOD } 4$ or $(0+d+k) \text{ MOD } 4$.

To ensure that the acquisition preamble (68,5) always ends in the desired phase state (such as two positive samples or two negative samples), the state of the precoder 10 is initialized to an appropriate value when writing the preamble (68,5) to the disk. For a PR4 read channel, for example, the delay registers in the $1/1+D^2$ precoder 10 are initialized to zero and an even number of 1 bits are output by the data generator 4 to ensure that the preamble ends in either two positive samples or two negative samples.

Enabling the data/servo sync mark detector A120 at every other sample period aids in the computer search for the optimum fault tolerant sync mark. The search program can search for minimum correlation between the sync mark and shifted versions of the sync mark concatenated with the preamble at every other shift rather than at every shift. This increases the probability of finding a sync mark having a higher degree of fault tolerance.

The sync mark detection technique of the present invention can be easily extended to search for the sync mark at every fourth sample period rather than at every other sample period. This requires that the preamble always end in the same two sample values (i.e., the preamble ends with the counter C128 in one out of the four possible states). Further, this technique can easily be extended for use with other preamble formats (e.g., 3T, 4T, 6T, etc) and with other types of PR read channels (e.g., EPR4 and EEPR4).

In an alternative embodiment of the present invention shown in Figure C6, the data/servo sync mark detector A120 processes two bits of the detected sequence 33 at a time. The target sync mark C102 is separated into an even and odd interleave and stored in an even register C150 and an odd register C152, respectively. Control logic C140 loads the even and odd interleaves (C142,C144) of the detected sequence 33 into respective shift registers (C146,C148) in response to an enable signal C194 from counter decode logic C190. The control logic C140 delays loading the shift registers (C146,C148) with the detected sequence 33 until the counter C128 of Figure C5B is in one of the two enabling

states $((2+d) \text{ MOD } 4 \text{ or } (0+d) \text{ MOD } 4)$.

In yet another embodiment of the present invention, the data/servo sync mark detector A120 correlates estimated sample values with expected sample values that corresponded to the target sync mark. For the purpose of this disclosure, then, the data/servo sync mark detector A120 is specified, in general, as generating channel values in response to the discrete time sample values and correlating the channel values with target values of a target sync mark.

The estimated and expected sample values of the detected and target sync mark are represented by Partial Response Class-IV (PR4) signals. The discrete time sequence detector 34 of Figure A3 outputs a sign and magnitude of the detected binary sequence (i.e., a two bit wide sequence). The signed binary output sequence is then encoded into a PR4 signal of estimated sample values. If the discrete time sequence detector 34 is a PR4 detector, then the signed binary output sequence is already in the PR4 format with the estimated samples normalized to $(-1, 0, +1)$. If the discrete time sequence detector 34 is an EPR4 or EEPR4 detector, then the output of the detector (NRZI format) is converted into a PR4 signal by passing the sign and magnitude bits through a $(1+D)$ filter as shown in Figure C7. Once in the PR4 representation, the sync mark detector computes a squared error between the detected PR4 sync mark and the target PR4 sync mark. When the squared error falls below a predetermined programmable threshold T_h , the sync mark has been detected.

Mathematically, the squared error signal is computed according to:

$$e^2 = (S_k - t_k)^2 = S_k^2 - 2 \cdot S_k \cdot t_k + t_k^2 \text{ where:}$$

S_k is the sign and magnitude of the estimated sample values; and

t_k is the sign and magnitude of the target sample values.

Since the polarity of the write signal may be opposite that of the read signal, the computed error signal is:

$$e^2 = S_k^2 - 2 \cdot \text{COR} + t_k^2 \quad \text{where:}$$

COR is either $+2S_k \cdot t_k$ or $-2S_k \cdot t_k$ depending on the polarity of the read signal as determined

by the timing recovery control signal C138 of Figure C5B.

The term ${}^2t_k^2$ equals the number of ones in the target sync mark, a constant.

Therefore, the test for the sync mark becomes:

$${}^2S_k^2 - 2 \cdot \text{COR} < \text{Th}'; \text{ where:}$$

Th' is a programmable threshold = $\text{Th} - {}^2t_k^2$.

The term ${}^2S_k^2$ equals the number of ones in the estimated samples and can be computed by counting the number of ones input into the sync mark detector. By initializing a counter with $-\text{Th}'$, incrementing the counter for each one input into the sync mark detector, and decrementing the counter with each one output from the detector, the content CNT of the counter is:

$${}^2S_k^2 - \text{Th}'. \quad (1)$$

The test for the sync mark is then:

$$2 \cdot \text{COR} > \text{CNT}. \quad (2)$$

A circuit for implementing equations (1) and (2) is illustrated in Figure C8. A 9-bit target sync mark 010010001 has been selected for the purpose of illustration, but other sync mark lengths and values are equally applicable. The circuit of Figure C8 assumes that the preamble always ends in two negative samples resulting in PR4 sample values for the target sync mark of 0+00+000-. If the preamble ends in two positive samples, then the PR4 values for the target sync mark are 0-00-000+ and the correlation is negated as described below.

Referring now to Figure C8, the PR4 sign and magnitude bits from the discrete time sequence detector 34 are input into control logic C140 similar to that of Figure C6. The control logic C140, responsive to a control signal C194 from counter decode logic C190, delays loading the shift registers with the PR4 data until the counter C128 of Figure C5B is in one of the enabling states as described above.

In order to implement the COR function of equation (2), an adder C160 adds the estimated PR4 values corresponding to the non-zero target PR4 values. Since the last target PR4 value is a "-1" when the preamble ends in two negative samples, an AND gate

C162 negates the last bit of the estimated PR4 values. A multiplying circuit C164 multiplies the COR signal by 2, and a multiplexor C166, responsive to the decoded timing recovery control signal C192, selects between an unmodified or a negated $2 \cdot \text{COR}$ signal (i.e., multiplied by -1 C188) depending on whether the preamble ends in - or ++, respectively. That is, the control signal C192 from the counter decode logic C190 will negate the correlation signal C186 when the output of the timing recovery counter C128 equals $(0+d+k) \text{ MOD } 4$ which corresponds to the preamble ending in two positive samples (i.e., the target PR4 sample values are 0-00-000+).

The circuit C168 for generating the CNT threshold value of equation (1) operates as follows. First, a storage register C170 is loaded with a predetermined programmable threshold -Th' C172 through a multiplexor C174, and the sync mark detector shift registers are cleared. Then for each clock cycle, counter logic C176 counts the number of non-zero values entering the sync mark detector and subtracts the number of non-zero values exiting the sync mark detector. The output of counter logic C176 (which can take on the values $\{0, \pm 1, \pm 2\}$) is input into an adder C178, added to the content of the storage register C170, and restored to the storage register C170 through multiplexor C174.

To complete the implementation of equation (2), the storage register C170, which contains the CNT value C180 of equation (1), is compared to the $2 \cdot \text{COR}$ value C182 at the output of the multiplexor C166 using a comparator C184. The output of the comparator C184 is the output C114 of the sync mark detector.

Figure C9 illustrates yet another embodiment of the sync mark detector which correlates the PR4 representation of the detected and target sync marks independent of the timing recovery expected sample generator B151 (i.e., independent of the counter C128). In this embodiment, a preamble synthesizer C196 generates the input control signal C194 and the sign control signal C192 in response to the recorded preamble. The preamble synthesizer C196 locks onto the recorded preamble sequence and then generates the 2T preamble independent of the sampled input sequence. Operation of the preamble synthesizer C196 is understood with reference to Figure C10.

In Figure C10, a counter C208 is cleared and a first shift register C202 is initialized

with the sequence 1,1,0,0,1,1,...,0,0 which corresponds to the PR4 sign bit sequence of the 2T preamble. The PR4 sign bit C200 from the sequence detector 34 is then input into a second shift register C204 and correlated with the first shift register C202 using an adder C206 and exclusive-nor gates not shown. The output of the adder C206 is compared to a predetermined threshold using a comparator C210. When the correlation exceeds the predetermined threshold, the preamble synthesizer has locked onto the recorded preamble. The counter C208 is enabled and clocked at each sample period to generate the sync mark detector input enable signal C194 and the sign control signal C192 through counter decode logic C190. Operation of the counter decode logic C190 is as described above except that it does not need to compensate for the delay associated with the equalizing filter 26 and sequence detector 34. That is, the input enable signal C194 is active when the output of the counter C208 is 00 or 10, and the sign control signal C192 is active when the output of the counter C208 is $(0+k) \text{ MOD } 4$. The C0 output of counter C208 is also shifted into the first shift register C202 so that the preamble synthesizer C196 continues to track the recorded 2T preamble. In this manner, the preamble synthesizer filters out errors in the detected 2T preamble caused by noise in the channel.

The operation of the data/servo sync mark detector A120 can be described mathematically by the following equation:

$$Y(k) = ([t_0, t_1, \dots, t_{N-1}] \cdot [S_k, S_{k+1}, \dots, S_{k+N-1}]^t \cdot I) > Th; \text{ where:}$$

$Y(k)$: output C114 of the data/servo sync mark detector A120;

k : the sample value index;

$[t_0, t_1, \dots, t_{N-1}]$: the target values of the target sync mark;

$[S_k, S_{k+1}, \dots, S_{k+N-1}]$: the channel values;

N : length of the target sync mark;

I : a sample period interval enable signal that is equal to 1 when $k \text{ modulo } Q$ is a member of a set S and 0 otherwise, where Q is a predetermined integer not equal to 1; and

Th : a predetermined threshold.

For the 2T acquisition preamble (68,5) described in the above examples where the output of the data/servo sync mark detector A120 is enabled at every other sample value, $Q=2$ and the set $S=\{0\}$.

Many changes in form and detail could be made without departing from the spirit and scope of the present invention; the particular embodiments disclosed herein are not intended to be limiting. The scope of the invention is properly construed from the following claims.

Table 1

Channel	Transfer Function	Dipulse Response
PR4	$(1-D)(1+D)$	0, 1, 0, -1, 0, 0, 0, ...
EPR4	$(1-D)(1+D)^2$	0, 1, 1, -1, -1, 0, 0, ...
EEPR4	$(1-D)(1+D)^3$	0, 1, 2, 0, -2, -1, 0, ...

Table B2

Sample Value	Slider Output
$y \geq T1$	+1
$-T2 \leq y < T1$	0
$y < -T2$	-1

Table C2

State	$Y(n-1)$	$Y(n)$	C1C0
+A,-A	+y	+y	00
-A,-A	+y	-y	01
-A,+A	-y	-y	10
+A,+A	-y	+y	11

We claim:

1. A sampled amplitude read channel for reading data from a magnetic medium by detecting digital data from a sequence of discrete time sample values generated by sampling pulses in an analog read signal from a magnetic read head positioned over the magnetic medium, comprising:
 - (a) a sampling device for generating the sequence of discrete time sample values;
 - (b) a discrete time sequence detector, responsive to the discrete time sample values, for outputting a magnitude and sign of estimated sample values corresponding to the detected digital data; and
 - (c) a sync mark detector for detecting a recorded sync mark by comparing the magnitude and sign of the estimated sample values to a magnitude and sign of target sample values of a target sync mark.
2. The sampled amplitude read channel as recited in claim 1, wherein:
 - (a) the fault tolerant sync mark detector compares the estimated sample values to the target sample values according to a predetermined sample period interval enable signal I ;
 - (b) I is 1 when k modulo Q is a member of a set S and 0 otherwise; and
 - (c) k is a sample value index and Q is a predetermined integer not equal to 1.
3. The sampled amplitude read channel as recited in claim 2, wherein the predetermined sample period interval enable signal I is 1 at every other sample period.
4. The sampled amplitude read channel as recited in claim 2, wherein $Q=2$ and the set $S=\{0\}$.
5. The sampled amplitude read channel as recited in claim 2, wherein the comparison

is a correlation and an output of the sync mark detector $Y(k)$ is:

$$Y(k) = ([t_0, t_1, \dots, t_{N-1}] \cdot [S_k, S_{k+1}, \dots, S_{k+N-1}]^t \cdot I) > Th; \text{ where:}$$

$[t_0, t_1, \dots, t_{N-1}]$ are target values of the target sync mark;

$[S_k, S_{k+1}, \dots, S_{k+N-1}]$ are the channel values;

N is a length of the target sync mark; and

Th is a predetermined threshold.

6. The sampled amplitude read channel as recited in claim 5, wherein $t_i \cdot S_{k+i} = 1$ if t_i equals S_{k+i} and $t_i \cdot S_{k+i} = 0$ if t_i does not equal S_{k+i} .
7. The sampled amplitude read channel as recited in claim 1, wherein a length of the target sync mark is programmable.
8. The sampled amplitude read channel as recited in claim 1, wherein:
 - (a) the sync mark detector compares an error signal to a threshold; and
 - (b) the error signal is computed proportional to:

$$\sum (S_k - t_k)^2 \text{ where:}$$

S_k is the sign and magnitude of the estimated sample values; and

t_k is the sign and magnitude of the target sample values.
9. The sampled amplitude read channel as recited in claim 8, wherein the threshold is programmable.
10. The sampled amplitude read channel as recited in claim 8, further comprising an acquisition preamble synthesizer for synthesizing a control signal phase locked to an acquisition preamble recorded on the magnetic medium, wherein the error signal is computed using the control signal.

11. The sampled amplitude read channel as recited in claim 10, wherein the control signal determines the sign of the target sample values.
12. The sampled amplitude read channel as recited in claim 10, wherein the acquisition preamble synthesizer comprises a state machine wherein a current state of the state machine generates the control signal.
13. The sampled amplitude read channel as recited in claim 12, wherein the state machine is a counter.
14. The sampled amplitude read channel as recited in claim 8, further comprising a timing recovery circuit having an expected sample value generator for acquiring an acquisition preamble recorded on the magnetic medium, wherein the error signal is computed using a control signal from the expected sample value generator.
15. The sampled amplitude read channel as recited in claim 1, wherein the sync mark detector processes in parallel an even and odd interleave of the estimated sample values.
16. The sampled amplitude read channel as recited in claim 1, wherein the discrete time sequence detector is a partial response detector selected from the group consisting of PR4, EPR4 and EEPR4.
17. The sampled amplitude read channel as recited in claim 1, wherein the discrete time sequence detector comprises a first and second sliding threshold detector for processing in parallel an even and odd interleave of the discrete time sample values, respectively.
18. The sampled amplitude read channel as recited in claim 1, wherein the discrete

time sequence detector generates signed NRZI data and encodes the signed NRZI data into the estimated sample values according to a partial response spectrum.

19. The sampled amplitude read channel as recited in claim 18, wherein the discrete time sequence detector is selected from the group consisting of EPR4 and EEPR4 and the partial response spectrum is PR4.
20. A fault tolerant method for detecting a sync mark recorded on a magnetic medium using a sampled amplitude read channel that reads digital data from the magnetic medium by detecting the digital data from a sequence of discrete time sample values generated by sampling pulses in an analog read signal from a magnetic read head positioned over the magnetic medium, comprising the steps of:
 - (a) sampling the analog read signal to generate the sequence of discrete time sample values;
 - (b) detecting, from the discrete time sample values, a magnitude and sign of estimated sample values corresponding to the detected digital data; and
 - (c) detecting the recorded sync mark by comparing the magnitude and sign of the estimated sample values to a magnitude and sign of target sample values of a target sync mark.
21. The fault tolerant method for detecting a sync mark as recited in claim 20, further comprising the step of comparing the estimated sample values to the target sample values according to a predetermined sample period interval enable signal I , wherein:
 - (a) I is 1 when k modulo Q is a member of a set S and 0 otherwise; and
 - (b) k is a sample value index and Q is a predetermined integer not equal to 1.
22. The fault tolerant method for detecting a sync mark as recited in claim 21, wherein the predetermined sample period interval enable signal I is 1 at every other sample

period.

23. The fault tolerant method for detecting a sync mark as recited in claim 21, wherein $Q=2$ and the set $S=\{0\}$.
24. The fault tolerant method for detecting a sync mark as recited in claim 21, wherein the step of comparing comprises a correlation:

$$Y(k) = ([t_0, t_1, \dots, t_{N-1}] \cdot [S_k, S_{k+1}, \dots, S_{k+N-1}]^t \cdot I) > Th;$$
 where:
 $[t_0, t_1, \dots, t_{N-1}]$ are target values of the target sync mark;
 $[S_k, S_{k+1}, \dots, S_{k+N-1}]$ are the channel values;
 N is a length of the target sync mark; and
 Th is a predetermined threshold.
25. The fault tolerant method for detecting a sync mark as recited in claim 24, wherein $t_i \cdot S_{k+i} = 1$ if t_i equals S_{k+i} and $t_i \cdot S_{k+i} = 0$ if t_i does not equal S_{k+i} .
26. The fault tolerant method for detecting a sync mark as recited in claim 20, wherein a length and a value of the target sync mark is programmable.
27. The fault tolerant method for detecting a sync mark as recited in claim 20, further comprising the steps of:
 - (a) computing an error signal proportional to:

$$\sum (S_k - t_k)^2$$
 where:
 S_k is the sign and magnitude of the estimated sample values; and
 t_k is the sign and magnitude of the target sample values; and
 - (b) comparing the error signal to a threshold.
28. The fault tolerant method for detecting a sync mark as recited in claim 27, wherein

the threshold is programmable.

29. The fault tolerant method for detecting a sync mark as recited in claim 27, further comprising the steps of:
 - (a) generating a control signal while acquiring an acquisition preamble recorded on the magnetic medium; and
 - (b) computing the error signal using the control signal.
30. The fault tolerant method for detecting a sync mark as recited in claim 29, further comprising the step of using the control signal to set the sign of a computed correlation between the estimated sample values and the target sample values.
31. The fault tolerant method for detecting a sync mark as recited in claim 29, wherein a timing recovery circuit generates expected sample values $X(n)$ used to acquire the acquisition preamble.
32. The fault tolerant method for detecting a sync mark as recited in claim 31, wherein:
 - (a) the expected sample values are generated by a state machine; and
 - (b) a current state of the state machine generates the control signal.
33. The fault tolerant method for detecting a sync mark as recited in claim 32, wherein the state machine is a counter.
34. The fault tolerant method for detecting a sync mark as recited in claim 20, wherein the step of detecting the recorded sync mark comprises the step of processing in parallel an even and odd interleave of the estimated sample values.
35. The fault tolerant method for detecting a sync mark as recited in claim 20, wherein the step of detecting the magnitude and sign of the estimated sample values

comprises a partial response detector selected from the group consisting of PR4, EPR4 and EEPR4.

36. The fault tolerant method for detecting a sync mark as recited in claim 20, wherein the step of detecting the magnitude and sign of the estimated sample values comprises a first and second sliding threshold detector for processing in parallel an even and odd interleave of the discrete time sample values, respectively.
37. The fault tolerant method for detecting a sync mark as recited in claim 20, further comprising the steps of:
 - (a) detecting signed NRZI data from the discrete time sample values;
 - (b) encoding the signed NRZI data into partial response data; and
 - (c) detecting the recorded sync mark from the partial response data.
38. A fault tolerant sync mark detector for detecting a recorded sync mark from a sequence of discrete time sample values generated by sampling pulses in an analog read signal from a magnetic read head position over a magnetic medium, comprising a comparator for comparing a sign and magnitude of channel values generated in response to the discrete time sample values to a sign and magnitude of target values of a target sync mark.
39. A fault tolerant method for detecting a recorded sync mark from a sequence of discrete time sample values generated by sampling pulses in an analog read signal from a magnetic read head position over a magnetic medium, comprising the step of comparing a sign and magnitude of channel values generated in response to the discrete time sample values to a sign and magnitude of target values of a target sync mark.

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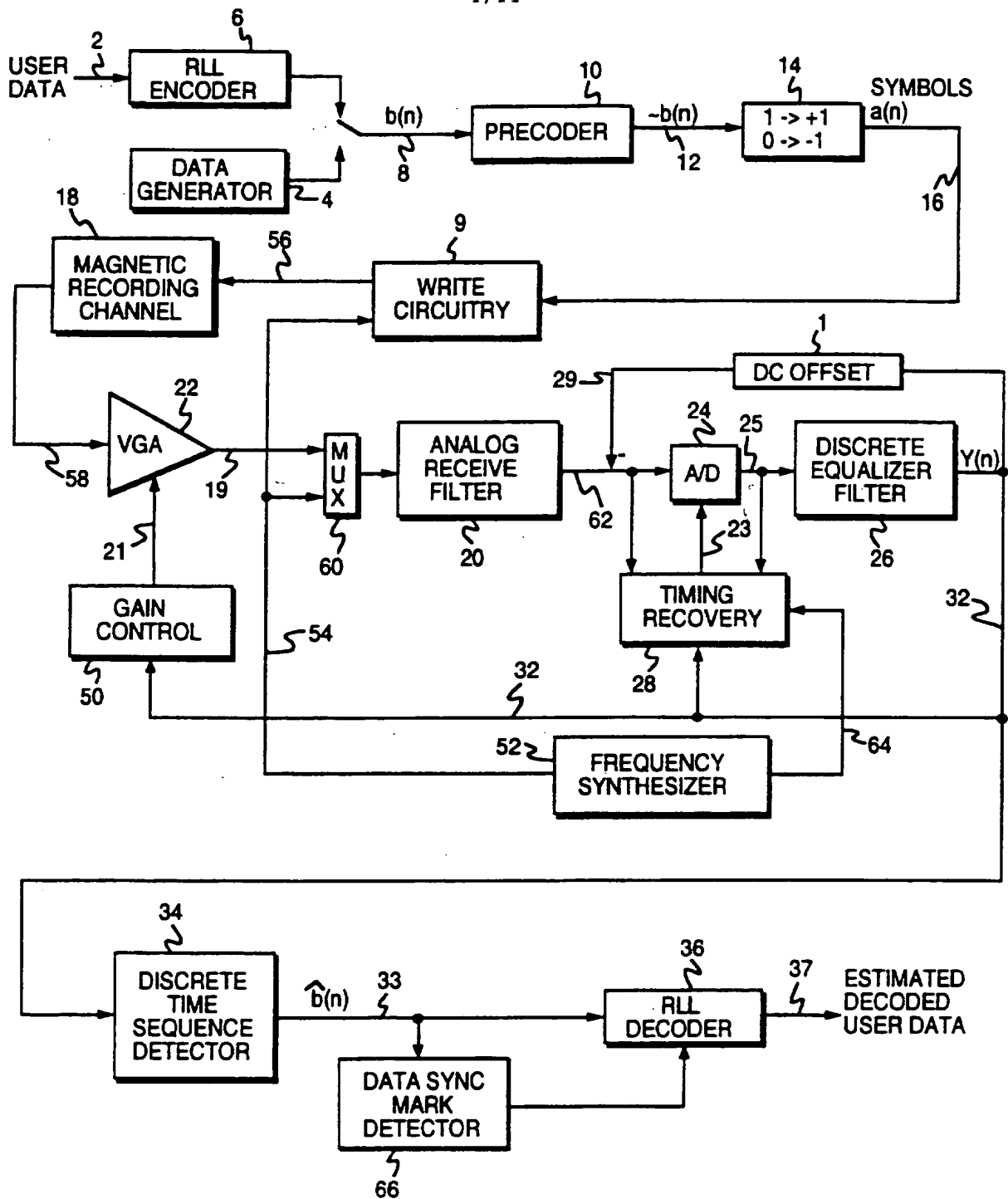


FIG. 1
(Prior Art)

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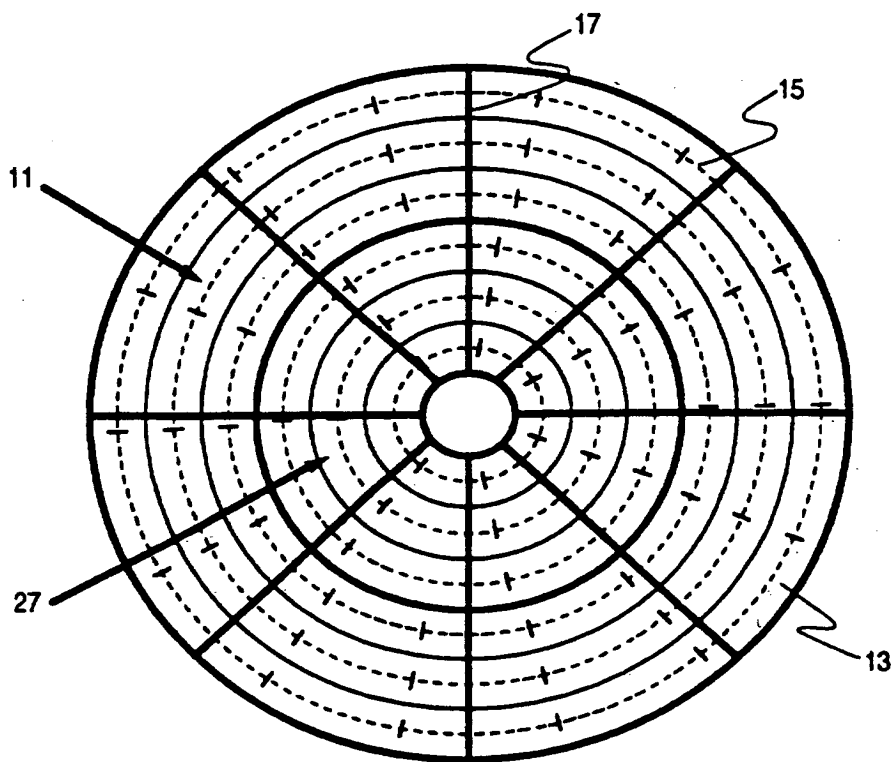


FIG. 2A
(Prior Art)

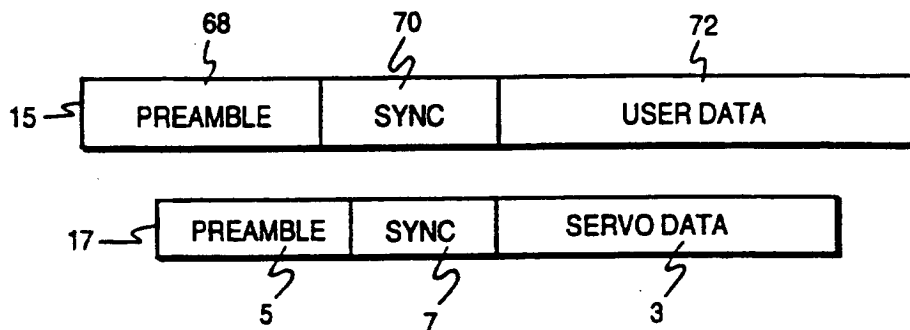


FIG. 2B
(Prior Art)

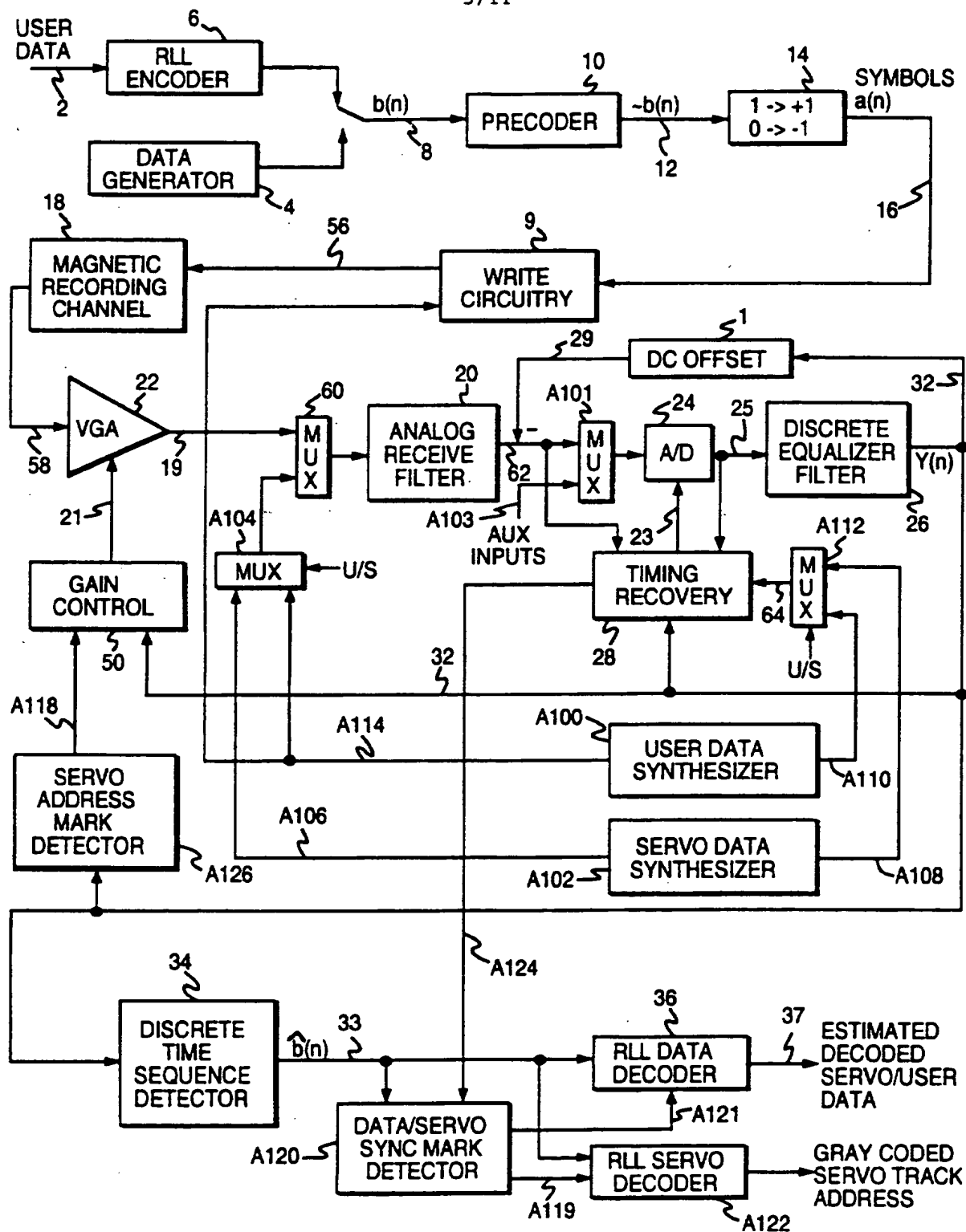


FIG. A3

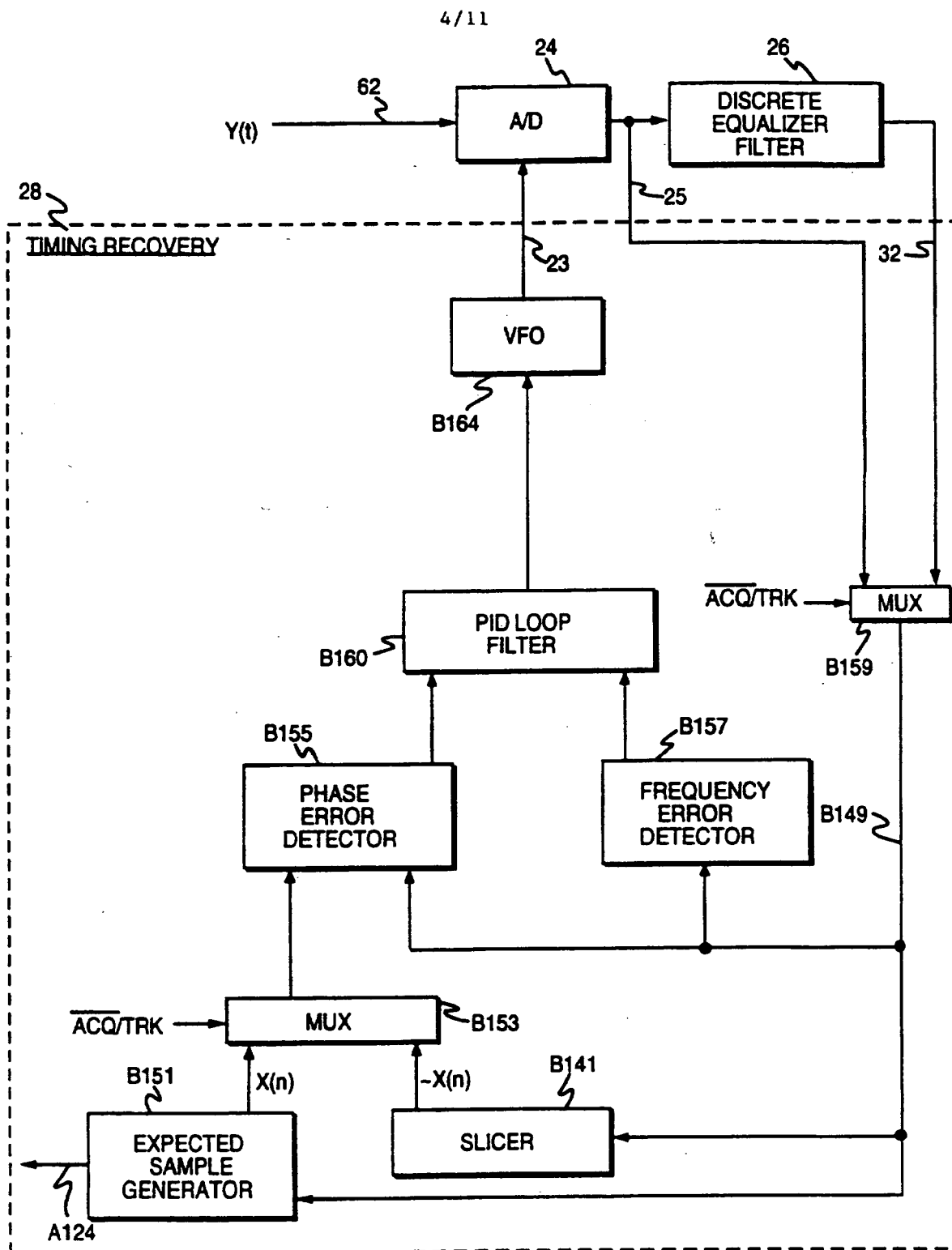


FIG. C3

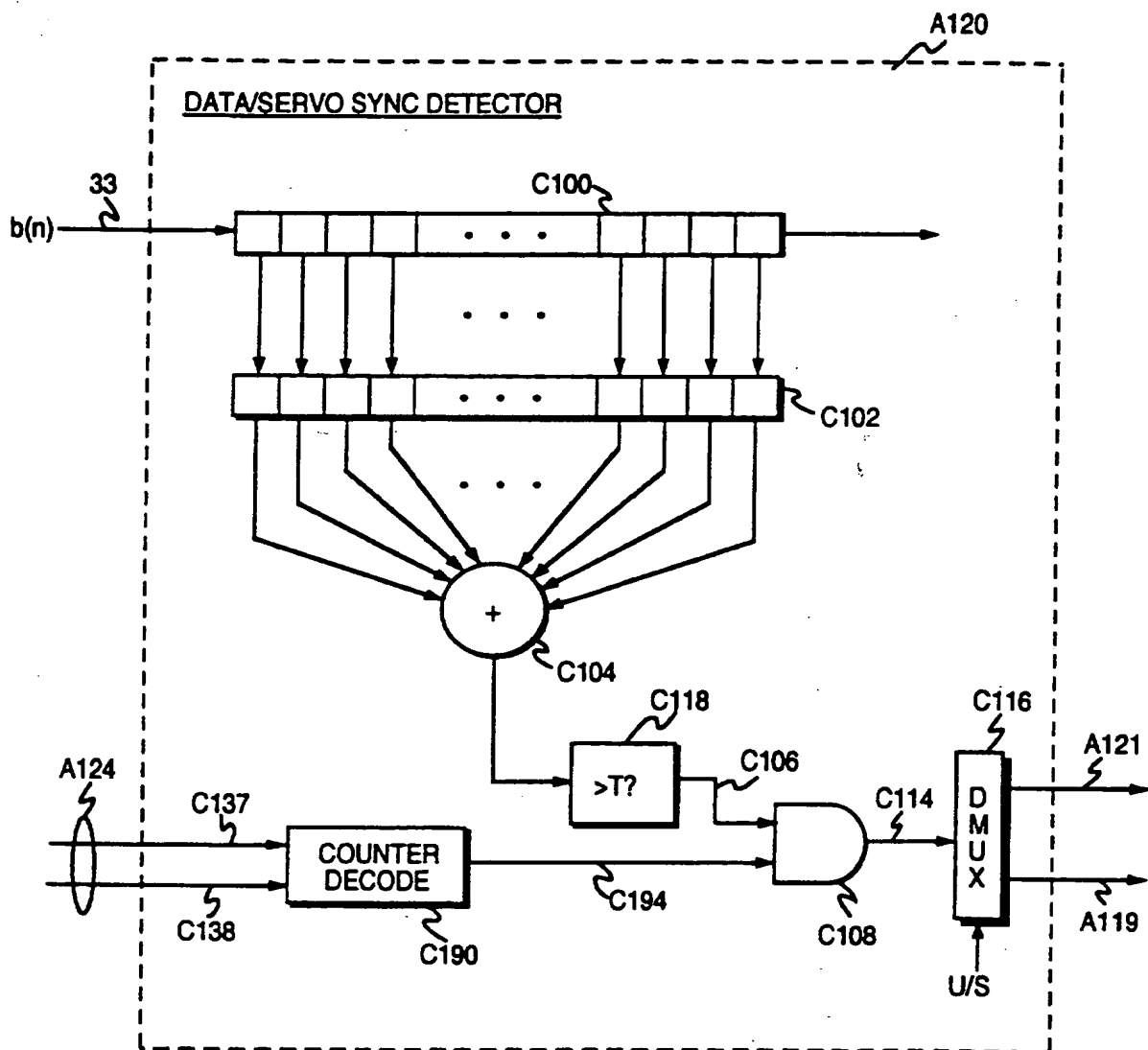


FIG. C4

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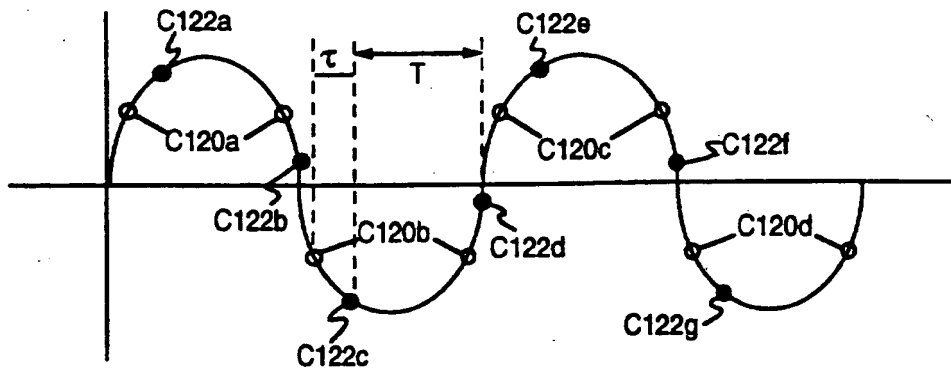


FIG. C5A

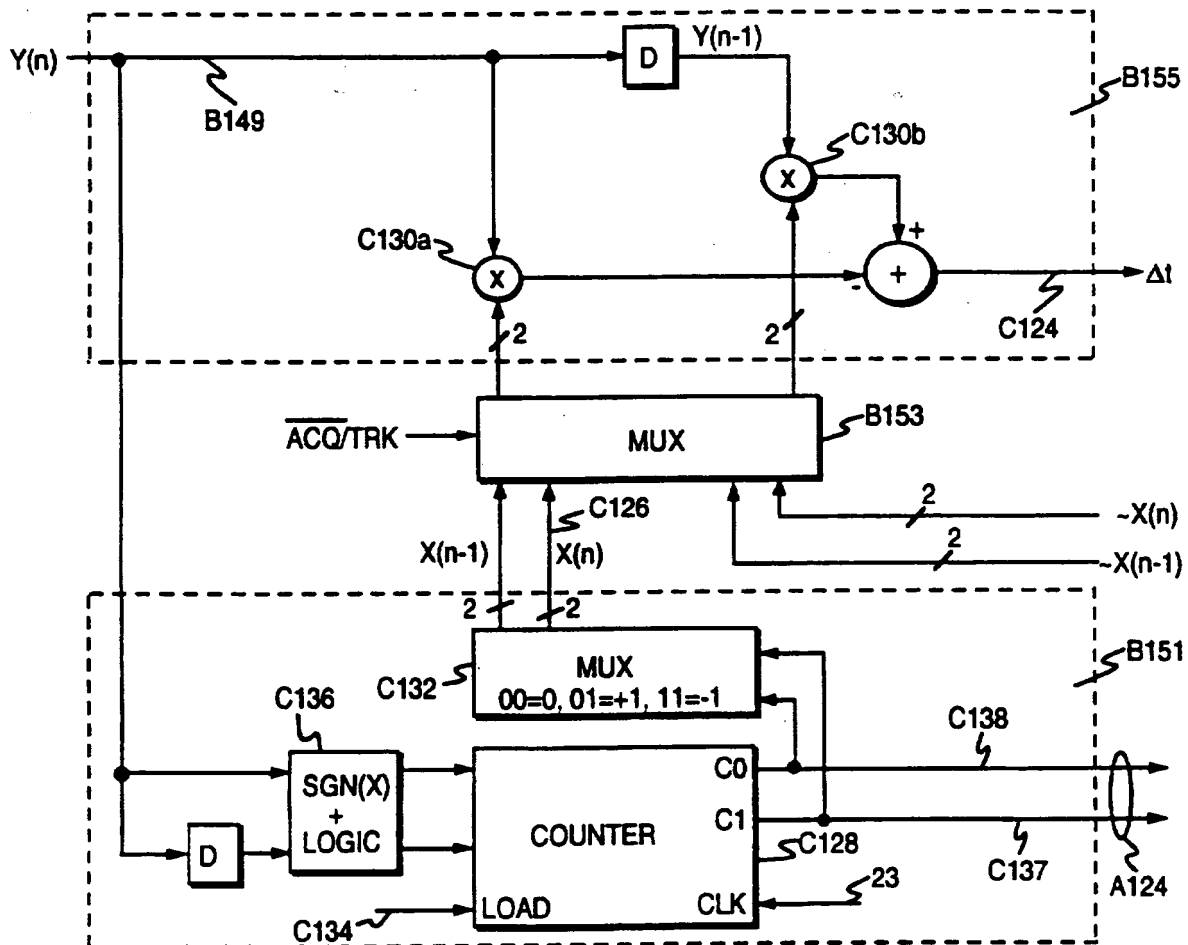


FIG. C5B

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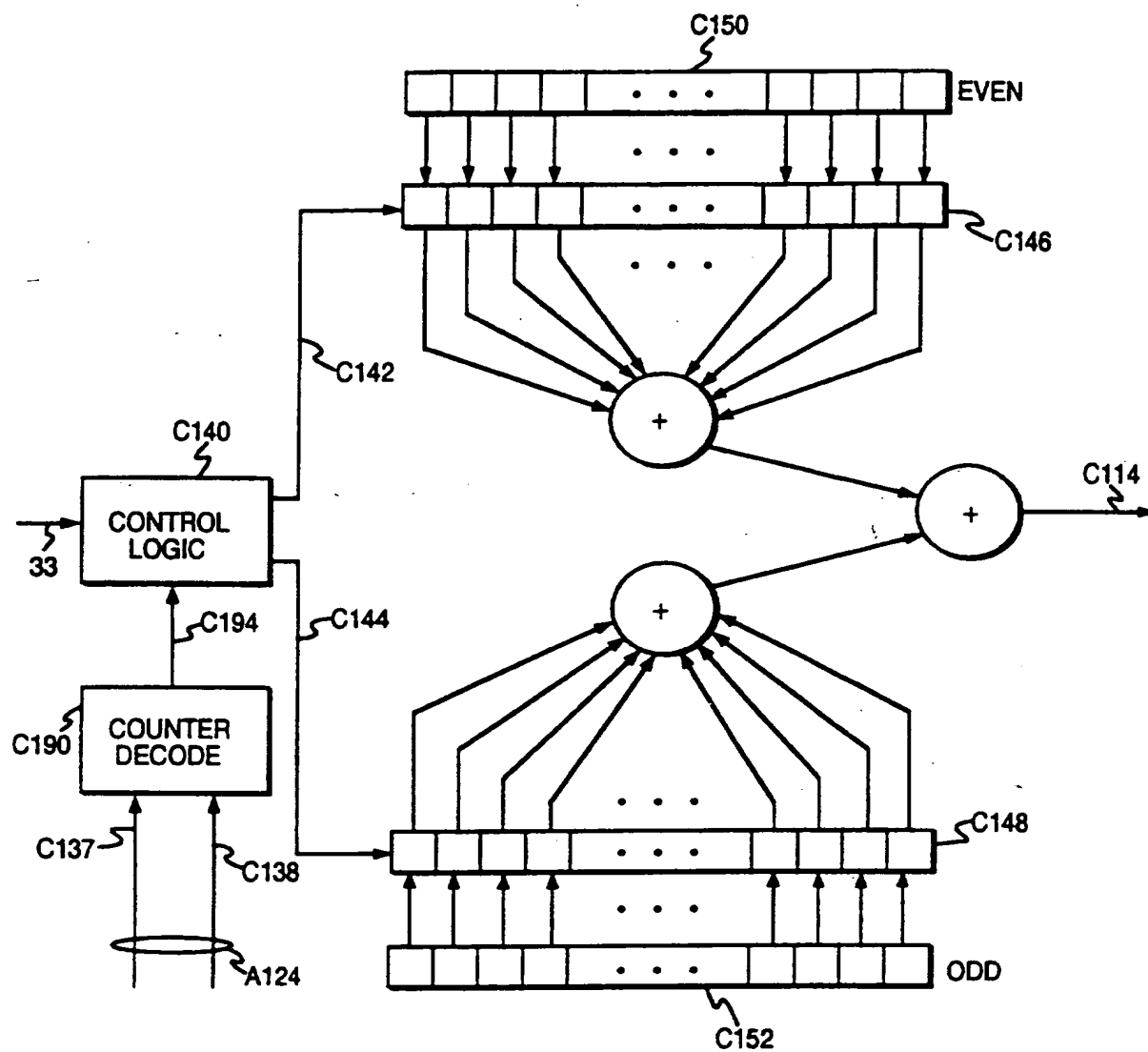


FIG. C6

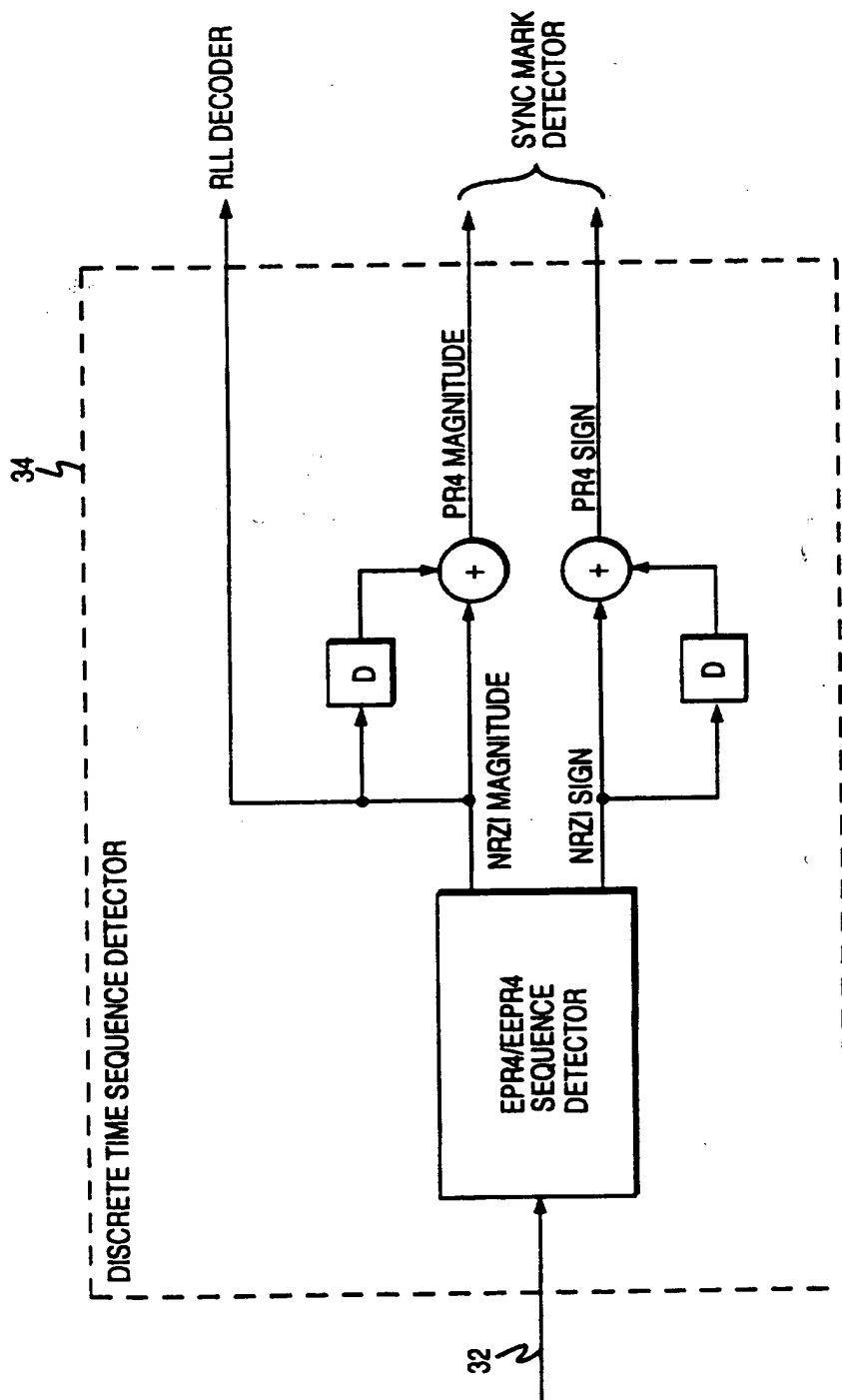


FIG. C7

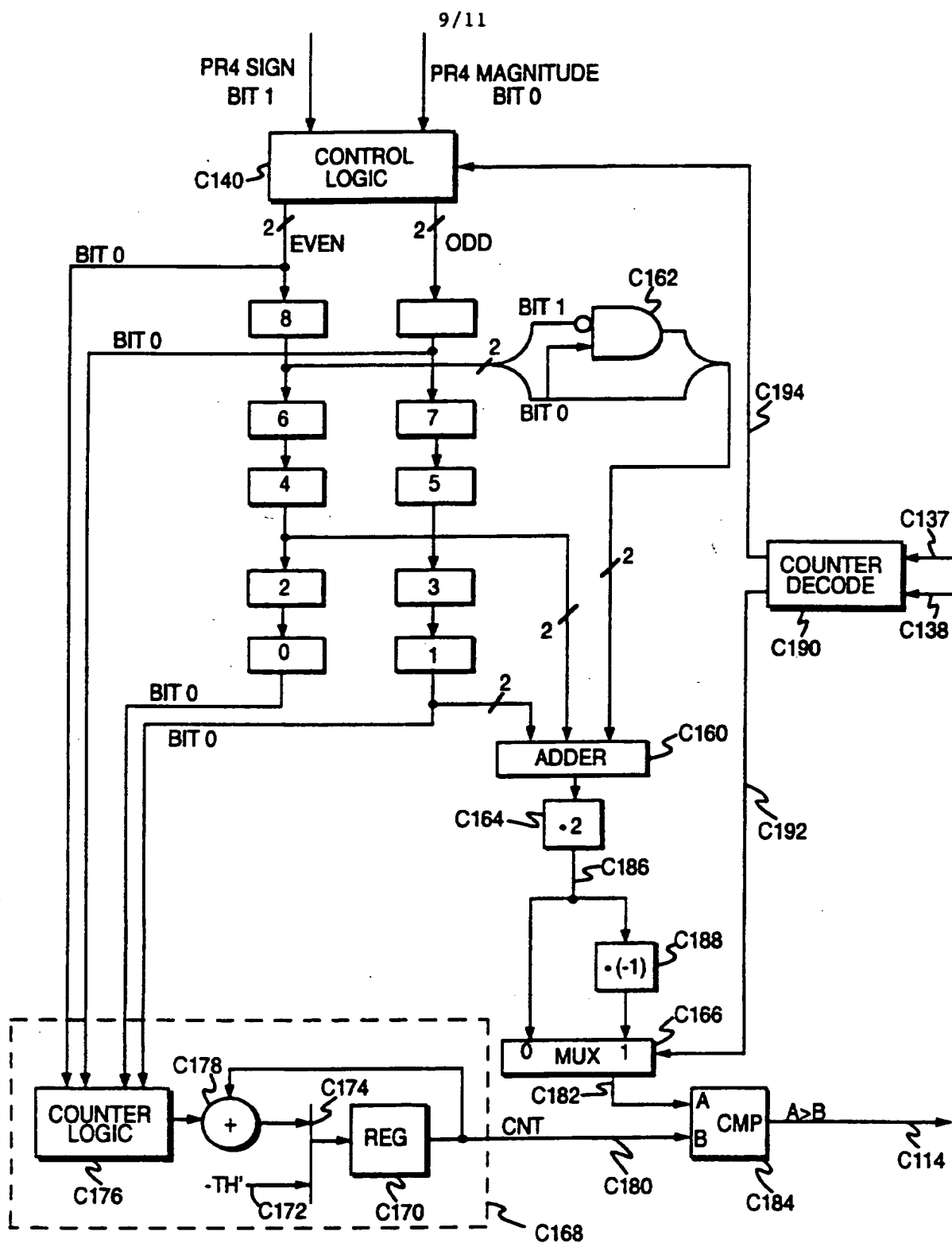


FIG. C8

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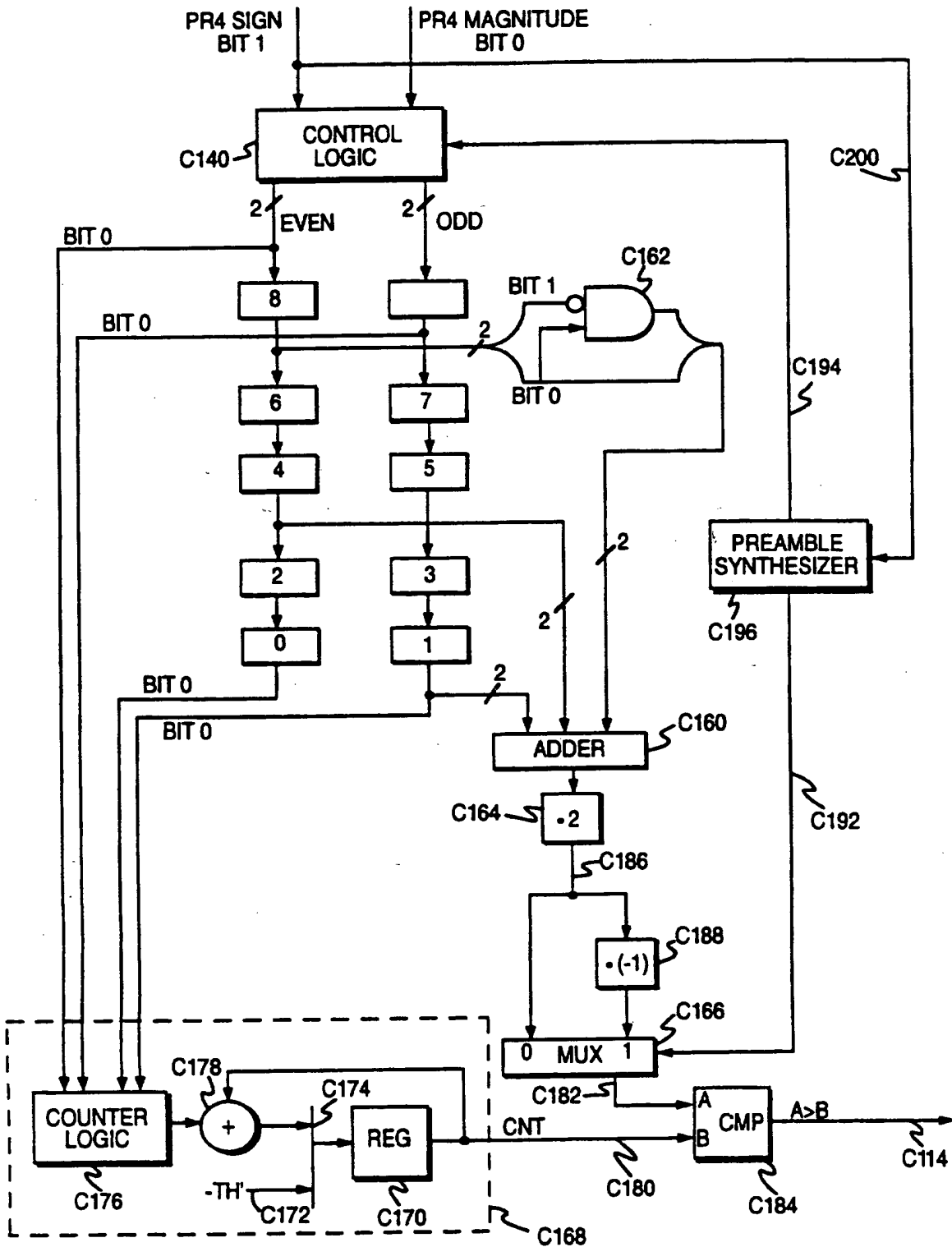


FIG. C9

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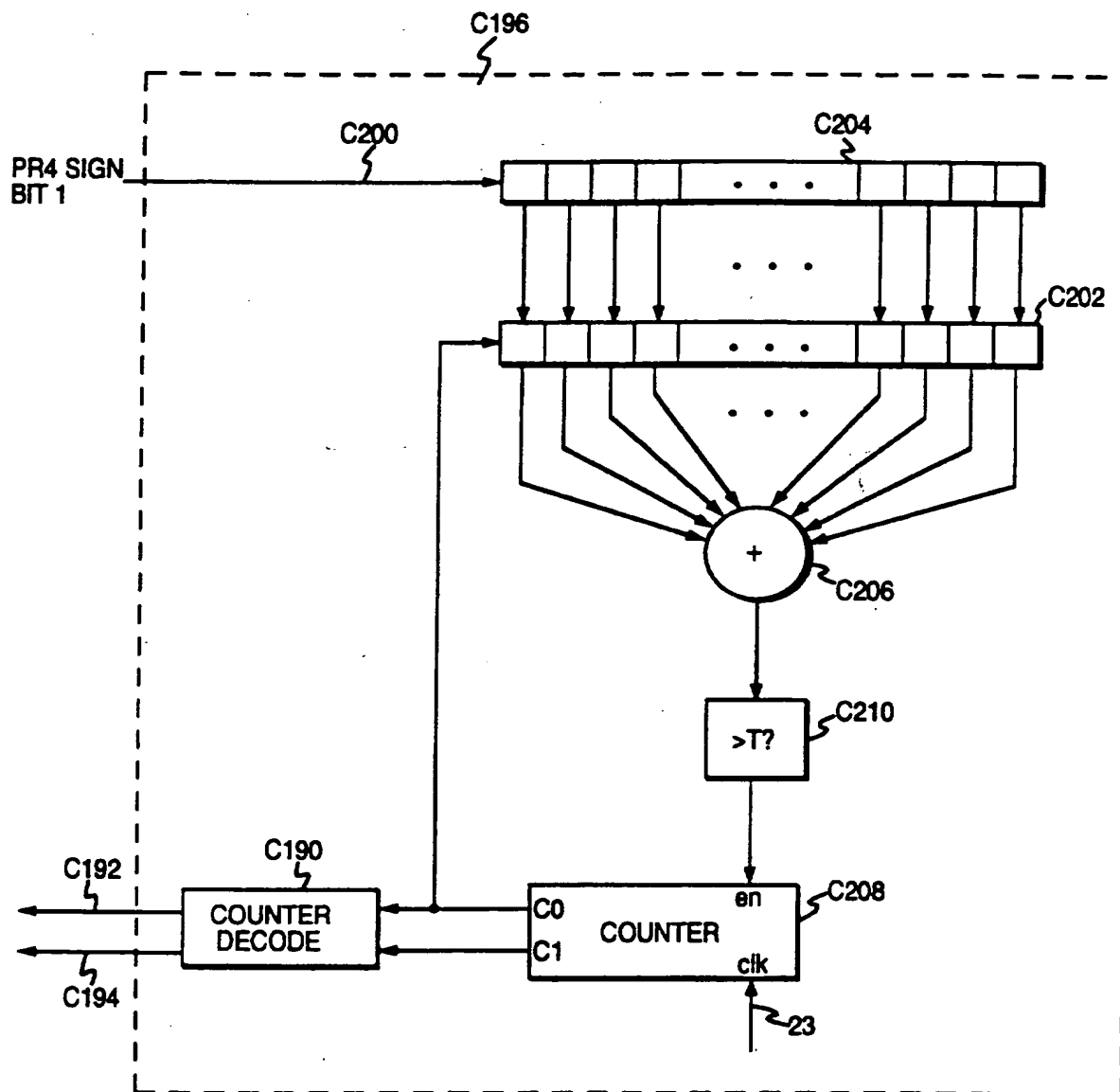


FIG. C10

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